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| 09/972,797 | 10/09/2001 | Dave Stuttard | 032658-018 | 3642 |

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GLENN PATENT GROUP
3475 EDISON WAY, SUITE L
MENLO PARK, CA 94025

| EXAMINER | |
|---|---|
| HUISMAN, DAVID J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/972,797 | STUTTARD ET AL. | |
| | Examiner | Art Unit | |
| | David J. Huisman | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 January 2006*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-205* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-205* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-7, 84-88, and 97-102, drawn to an array processor having one or more redundant blocks to replace a faulty block, classified in class 714, subclass 13.

II. Claims 8-11, drawn to an array processor having a mathematical expression evaluator in each processing block, classified in class 712, subclass 22.

III. Claims 12, 90-96, and 109, 111-112, drawn to an apparatus for separating instructions and data before they are supplied to processing blocks, classified in class 712, subclass 10.

IV. Claim 13, drawn to internal processing block data circulation, classified in class 712, subclass 18.

V. Claims 14, 60-67, and 122-132, drawn to processing elements comprising register files and memory for storing data to be processed and transferred to other elements, classified in class 712, subclass 14.

VI. Claims 15-17 and 113-119, drawn to a controller for controlling transfer of data between external memory and each processing element and calculating memory addresses via combination, classified in class 711, subclass 220.

VII. Claims 18-20 and 120-121, drawn to an enable register for indicating availability of a plurality of processing elements for processing, classified in class 712, subclass 16.

VIII. Claims 21-27 and 133-139, drawn to data transfer between neighboring elements within one processing block and between neighboring blocks, classified in class 712, subclass 11.

IX. Claims 28-31 and 140-149, drawn to combining a plurality of instruction streams into a serial stream and distributing that stream to a processing controller, classified in class 712, subclass 214.

X. Claims 32-39, 75-83, and 153-170, drawn to a semaphore controller for maintaining synchronism between execution of multiple instruction streams, classified in class 709, subclass 248.

XI. Claims 40-55 and 182-198, drawn to an array controller for routing instructions depending on the type of instruction, classified in class 712, subclass 22.

XII. Claims 56-59, 103-108, and 110, drawn to a segment register for each processing block, for storing information which indicates the address area of a local memory to be accessed by the corresponding processing block, classified in class 711, subclass 220.

XIII. Claims 68-70 and 150-152, drawn to scheduling instruction streams based on stream priority, classified in class 712, subclass 214.

XIV. Claims 71-74 and 199-205, drawn to memory unit accesses by a plurality of processor elements having access indicators, classified in class 711, subclass 154.

XV. Claims 171-181, drawn to a controller for transferring data to and from internal processing element memory independently of processor element operation, classified in class 712, subclass 16.

The inventions are distinct, each from the other because of the following reasons:

2. The inventions are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case:

1a) invention I has separate utility from invention II such as providing fault tolerance in any processing system and not just in a system that contains a plurality of processing elements with mathematical expression evaluators.

1b) invention I has separate utility from invention III such as providing fault tolerance in any processing system and not just in a system that requires instructions and data be separated.

1c) invention I has separate utility from invention IV such as providing fault tolerance in any processing system which does not depend on the claimed internal data circulation technique of invention IV.

1d) invention I has separate utility from invention V such as providing fault tolerance in any processing system which does not depend on the claimed register files and memory.

1e) invention I has separate utility from invention VI such as providing fault tolerance in any processing system and not just in a system with the claimed controller for controlling transfer of data to external memory and calculating memory addresses.

1f) invention I has separate utility from invention VII such as providing fault tolerance in any processing system. Fault tolerance can be provided in a system that does not include the claimed enable register for indicating availability of processing elements.

1g) invention I has separate utility from invention VIII such as providing fault tolerance in any processing system. Fault tolerance can be provided in systems that do not require the specifics of neighboring processor element transfer.

1h) invention I has separate utility from invention IX such as providing fault tolerance in any processing system and not just in a system which combines multiple instruction streams into a serial stream.

1i) invention I has separate utility from invention X such as providing fault tolerance in any processing system that does not include a semaphore controller for maintaining synchronism of execution of instruction streams.

1j) invention I has separate utility from invention XI such as providing fault tolerance in any processing system and not just in a system which has an array controller for routing instructions depending on the type of instruction.

1k) invention I has separate utility from invention XII such as providing fault tolerance in any processing system that does not have the claimed segment register for storing information as to what area of memory may be accessed by processing elements.

1l) invention I has separate utility from invention XIII such as providing fault tolerance in any processing system and not just in a system which schedules instruction streams based on priority of the streams.

1m) invention I has separate utility from invention XIV such as providing fault tolerance in any processing system not having the specific read/write memory access techniques of invention XIV.

1n) invention I has separate utility from invention XV such as providing fault tolerance in any processing system and not just in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.

2a) invention II has separate utility from invention III such as having each processing element evaluate mathematical expressions in any array processing system and not just in a system that requires instructions and data be separated.

2b) invention II has separate utility from invention IV such as having each processing element evaluate mathematical expressions in any array processing system which does not depend on the claimed internal data circulation technique of invention IV. That is, as long as data is presented in any way, and not in applicant's claimed way, mathematical expressions may be evaluated.

2c) invention II has separate utility from invention V such as having each processing element evaluate mathematical expressions in any array processing system which does not depend on the claimed register files and memory.

2d) invention II has separate utility from invention VI such as having each processing element evaluate mathematical expressions in any array processing system and not just in a system with the claimed controller for controlling transfer of data to external memory and calculating memory addresses.

2e) invention II has separate utility from invention VII such as having each processing element evaluate mathematical expressions in any array processing system. Mathematical expression evaluation can be provided in a system that does not include the claimed enable register for indicating availability of processing elements.

2f) invention II has separate utility from invention VIII such as having each processing element evaluate mathematical expressions in any array processing system. Mathematical expression evaluation can be provided in a system that does not require the specifics of neighboring processor element transfer. For instance, neighbors could not communicate at all, but an evaluation by any given one element may still occur.

2g) invention II has separate utility from invention IX such as having each processing element evaluate mathematical expressions in any array processing system and not just in a system which combines multiple instruction streams into a serial stream.

2h) invention II has separate utility from invention X such as having each processing element evaluate mathematical expressions in any array processing system that does not include a semaphore controller for maintaining synchronism of execution of instruction streams.

2i) invention II has separate utility from invention XI such as having each processing element evaluate mathematical expressions in any array processing system and not just in a system which has an array controller for routing instructions depending on the type of instruction.

2j) invention II has separate utility from invention XII such as having each processing element evaluate mathematical expressions in any array processing system that does not have the claimed segment register for storing information as to what area of memory may be accessed by processing elements.

2k) invention II has separate utility from invention XIII such as having each processing element evaluate mathematical expressions in any array processing system and not just in a system which schedules instruction streams based on priority of the streams.

2l) invention II has separate utility from invention XIV such as having each processing element evaluate mathematical expressions in any array processing system not having the specific read/write memory access techniques of invention XIV.

2m) invention II has separate utility from invention XV such as having each processing element evaluate mathematical expressions in any array processing system and not just in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.

3a) invention III has separate utility from invention IV such as separating instructions from data so that the portions may be operated on appropriately in any system which does not depend on the claimed internal data circulation technique of invention IV.

3b) invention III has separate utility from invention V such as separating instructions from data so that the portions may be operated on appropriately in any system which does not depend on the claimed register files and memory.

3c) invention III has separate utility from invention VI such as separating instructions from data so that the portions may be operated on appropriately in any system and not just in a system with the claimed controller for controlling transfer of data to external memory and calculating memory addresses.

3d) invention III has separate utility from invention VII such as separating instructions from data so that the portions may be operated on appropriately in any system. Separation can be provided in a system that does not include the claimed enable register for indicating availability of processing elements.

3e) invention III has separate utility from invention VIII such as separating instructions from data so that the portions may be operated on appropriately in any system. Separation can be provided in a system that does not require the specifics of neighboring processor element transfer.

3f) invention III has separate utility from invention IX such as separating instructions from data so that the portions may be operated on appropriately in any system and not just in a system which combines multiple instruction streams into a serial stream.

3g) invention III has separate utility from invention X such as separating instructions from data so that the portions may be operated on appropriately in any system that does not include a semaphore controller for maintaining synchronism of execution of instruction streams.

3h) invention III has separate utility from invention XI such as separating instructions from data so that the portions may be operated on appropriately in any system and not just in a system which has an array controller for routing instructions depending on the type of instruction.

3i) invention III has separate utility from invention XII such as separating instructions from data so that the portions may be operated on appropriately in any system that does not have the claimed segment register for storing information as to what area of memory may be accessed by processing elements.

3j) invention III has separate utility from invention XIII such as separating instructions from data so that the portions may be operated on appropriately in any system and not just in a system which schedules instruction streams based on priority of the streams.

3k) invention III has separate utility from invention XIV such as separating instructions from data so that the portions may be operated on appropriately in any system not having the specific read/write memory access techniques of invention XIV.

3l) invention III has separate utility from invention XV such as separating instructions from data so that the portions may be operated on appropriately in any system and not just in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.

4a) invention IV has separate utility from invention V such as internally circulating data among processor elements (to cut back on time spent at external circulation) in any system which does not depend on the claimed register files and memory.

4b) invention IV has separate utility from invention VI such as internally circulating data among processor elements (to cut back on time spent at external circulation) in any system and not just in a system with the claimed controller for controlling transfer of data to external memory and calculating memory addresses.

4c) invention IV has separate utility from invention VII such as internally circulating data among processor elements (to cut back on time spent at external circulation) in any system. Internal circulation can be provided in a system that does not include the claimed enable register for indicating availability of processing elements.

4d) invention IV has separate utility from invention VIII such as internally circulating data among processor elements (to cut back on time spent at external circulation) in any system. Internal circulation can be provided in a system that does not require the specifics of neighboring processor element transfer.

4e) invention IV has separate utility from invention IX such as internally circulating data among processor elements (to cut back on time spent at external circulation) in any system and not just in a system which combines multiple instruction streams into a serial stream.

4f) invention IV has separate utility from invention X such as internally circulating data among processor elements (to cut back on time spent at external circulation) in any system that does not include a semaphore controller for maintaining synchronism of execution of instruction streams.

4g) invention IV has separate utility from invention XI such as internally circulating data among processor elements (to cut back on time spent at external circulation) in any system and not just in a system which has an array controller for routing instructions depending on the type of instruction.

4h) invention IV has separate utility from invention XII such as internally circulating data among processor elements (to cut back on time spent at external circulation) in any system that does not have the claimed segment register for storing information as to what area of memory may be accessed by processing elements.

4i) invention IV has separate utility from invention XIII such as internally circulating data among processor elements (to cut back on time spent at external circulation) in any system and not just in a system which schedules instruction streams based on priority of the streams.

4j) invention IV has separate utility from invention XIV such as internally circulating data among processor elements (to cut back on time spent at external circulation) in any system not having the specific read/write memory access techniques of invention XIV.

4k) invention IV has separate utility from invention XV such as internally circulating data among processor elements (to cut back on time spent at external circulation) in any system and not just

in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.

5a) invention V has separate utility from invention VI such as providing register file and memory storage for processing elements in any system and not just in a system with the claimed controller for controlling transfer of data to external memory and calculating memory addresses. There are many different ways in which transfer may be controlled.

5b) invention V has separate utility from invention VII such as providing register file and memory storage for processing elements in any system. This storage can be provided in a system that does not include the claimed enable register for indicating availability of processing elements.

5c) invention V has separate utility from invention VIII such as providing register file and memory storage for processing elements in any system. This storage can be provided in a system that does not require the specifics of neighboring processor element transfer.

5d) invention V has separate utility from invention IX such as providing register file and memory storage for processing elements in any system and not just in a system which combines multiple instruction streams into a serial stream.

5e) invention V has separate utility from invention X such as providing register file and memory storage for processing elements in any system that does not include a semaphore controller for maintaining synchronism of execution of instruction streams.

5f) invention V has separate utility from invention XI such as providing register file and memory storage for processing elements in any system and not just in a system which has an array controller for routing instructions depending on the type of instruction.

5g) invention V has separate utility from invention XII such as providing register file and memory storage for processing elements in any system that does not have the claimed segment register for storing information as to what area of memory may be accessed by processing elements.

5h) invention V has separate utility from invention XIII such as providing register file and memory storage for processing elements in any system and not just in a system which schedules instruction streams based on priority of the streams.

5i) invention V has separate utility from invention XIV such as providing register file and memory storage for processing elements in any system not having the specific read/write memory access techniques of invention XIV.

5j) invention V has separate utility from invention XV such as providing register file and memory storage for processing elements in any system and not just in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.

6a) invention VI has separate utility from invention VII such as controlling transfer of data between external memory and each processing element and calculating memory addresses in any processing system that does not have to include the claimed enable register for indicating availability of processing elements.

6b) invention VI has separate utility from invention VIII such as controlling transfer of data between external memory and each processing element and calculating memory addresses in any processing system that does not require the specifics of neighboring processor element transfer.

6c) invention VI has separate utility from invention IX such as controlling transfer of data between external memory and each processing element and calculating memory addresses in any processing system and not just in a system which combines multiple instruction streams into a serial stream.

6d) invention VI has separate utility from invention X such as controlling transfer of data between external memory and each processing element and calculating memory addresses in any processing system that does not include a semaphore controller for maintaining synchronism of execution of instruction streams.

6e) invention VI has separate utility from invention XI such as controlling transfer of data between external memory and each processing element and calculating memory addresses in any processing system and not just in a system which has an array controller for routing instructions depending on the type of instruction.

6f) invention VI has separate utility from invention XII such as controlling transfer of data between external memory and each processing element and calculating memory addresses in any processing system that does not have the claimed segment register for storing information as to what area of memory may be accessed by processing elements.

6g) invention VI has separate utility from invention XIII such as controlling transfer of data between external memory and each processing element and calculating memory addresses in any processing system and not just in a system which schedules instruction streams based on priority of the streams.

6h) invention VI has separate utility from invention XIV such as controlling transfer of data between external memory and each processing element and calculating memory addresses in any

processing system not having the specific read/write memory access techniques of invention XIV.

6i) invention VI has separate utility from invention XV such as controlling transfer of data between external memory and each processing element and calculating memory addresses in any processing system and not just in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.

7a) invention VII has separate utility from invention VIII such as detecting availability of a plurality of processing elements for processing in any multiprocessor system that does not require the specifics of neighboring processor element transfer.

7b) invention VII has separate utility from invention IX such as detecting availability of a plurality of processing elements for processing in any multiprocessor system and not just in a system which combines multiple instruction streams into a serial stream.

7c) invention VII has separate utility from invention X such as detecting availability of a plurality of processing elements for processing in any multiprocessor system that does not include a semaphore controller for maintaining synchronism of execution of instruction streams.

7d) invention VII has separate utility from invention XI such as detecting availability of a plurality of processing elements for processing in any multiprocessor system and not just in a system which has an array controller for routing instructions depending on the type of instruction.

7e) invention VII has separate utility from invention XII such as detecting availability of a plurality of processing elements for processing in any multiprocessor system that does not have

the claimed segment register for storing information as to what area of memory may be accessed by processing elements.

7f) invention VII has separate utility from invention XIII such as detecting availability of a plurality of processing elements for processing in any multiprocessor system and not just in a system which schedules instruction streams based on priority of the streams.

7g) invention VII has separate utility from invention XIV such as detecting availability of a plurality of processing elements for processing in any multiprocessor system not having the specific read/write memory access techniques of invention XIV.

7h) invention VII has separate utility from invention XV such as detecting availability of a plurality of processing elements for processing in any multiprocessor system and not just in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.

8a) invention VIII has separate utility from invention IX such as transferring data between neighboring elements and blocks in a multiple processing element system and not just in a system which combines multiple instruction streams into a serial stream.

8b) invention VIII has separate utility from invention X such as transferring data between neighboring elements and blocks in a multiple processing element system that does not include a semaphore controller for maintaining synchronism of execution of instruction streams.

8c) invention VIII has separate utility from invention XI such as transferring data between neighboring elements and blocks in a multiple processing element system and not just in a system which has an array controller for routing instructions depending on the type of instruction.

8d) invention VIII has separate utility from invention XII such as transferring data between neighboring elements and blocks in a multiple processing element system that does not have the claimed segment register for storing information as to what area of memory may be accessed by processing elements.

8e) invention VIII has separate utility from invention XIII such as transferring data between neighboring elements and blocks in a multiple processing element system and not just in a system which schedules instruction streams based on priority of the streams.

8f) invention VIII has separate utility from invention XIV such as transferring data between neighboring elements and blocks in a multiple processing element system not having the specific read/write memory access techniques of invention XIV.

8g) invention VIII has separate utility from invention XV such as transferring data between neighboring elements and blocks in a multiple processing element system and not just in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.

9a) invention IX has separate utility from invention X such as combining multiple instructions streams into a single instruction stream so that the single stream may be handled and distributed by some single scheduler in any system that does not include a semaphore controller for maintaining synchronism of execution of instruction streams.

9b) invention IX has separate utility from invention XI such as combining multiple instructions streams into a single instruction stream so that the single stream may be handled and distributed by some single scheduler in any system and not just in a system which has an array controller for

routing instructions depending on the type of instruction. For instance, the routing may be done in some other manner on a combined stream (such as priority or dependency routing).

9c) invention IX has separate utility from invention XII such as combining multiple instructions streams into a single instruction stream so that the single stream may be handled and distributed by some single scheduler in any system that does not have the claimed segment register for storing information as to what area of memory may be accessed by processing elements.

9d) invention IX has separate utility from invention XIII such as combining multiple instructions streams into a single instruction stream so that the single stream may be handled and distributed by some single scheduler in any system and not just in a system which schedules instruction streams based on priority of the streams.

9e) invention IX has separate utility from invention XIV such as combining multiple instructions streams into a single instruction stream so that the single stream may be handled and distributed by some single scheduler in any system not having the specific read/write memory access techniques of invention XIV.

9f) invention IX has separate utility from invention XV such as combining multiple instructions streams into a single instruction stream so that the single stream may be handled and distributed by some single scheduler in any system and not just in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.

10a) invention X has separate utility from invention XI such as using semaphores to synchronize execution of multiple instruction streams to ensure correct execution in any system and not just

in a system which has an array controller for routing instructions depending on the type of instruction.

10b) invention X has separate utility from invention XII such as using semaphores to synchronize execution of multiple instruction streams to ensure correct execution in any system that does not have the claimed segment register for storing information as to what area of memory may be accessed by processing elements.

10c) invention X has separate utility from invention XIII such as using semaphores to synchronize execution of multiple instruction streams to ensure correct execution in any system and not just in a system which schedules instruction streams based on priority of the streams.

10d) invention X has separate utility from invention XIV such as using semaphores to synchronize execution of multiple instruction streams to ensure correct execution in any system not having the specific read/write memory access techniques of invention XIV.

10e) invention X has separate utility from invention XV such as using semaphores to synchronize execution of multiple instruction streams to ensure correct execution in any system and not just in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.

11a) invention XI has separate utility from invention XII such as routing certain types of instructions to certain types of units in any system that does not have the claimed segment register for storing information as to what area of memory may be accessed by processing elements.

11b) invention XI has separate utility from invention XIII such as routing certain types of instructions to certain types of units in any system and not just in a system which schedules instruction streams based on priority of the streams.

11c) invention XI has separate utility from invention XIV such as routing certain types of instructions to certain types of units in any system not having the specific read/write memory access techniques of invention XIV.

11d) invention XI has separate utility from invention XV such as routing certain types of instructions to certain types of units in any system and not just in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.

12a) invention XII has separate utility from invention XIII such as specifying an area of memory which may be accessed by a particular processing element in any system and not just in a system which schedules instruction streams based on priority of the streams.

12b) invention XII has separate utility from invention XIV such as specifying an area of memory which may be accessed by a particular processing element in any system not having the specific read/write memory access techniques of invention XIV.

12c) invention XII has separate utility from invention XV such as specifying an area of memory which may be accessed by a particular processing element in any system and not just in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.

13a) invention XIII has separate utility from invention XIV such as scheduling instruction streams based on priority (thereby allowing to get more important processes completed quicker) in any system not having the specific read/write memory access techniques of invention XIV.
13b) invention XIII has separate utility from invention XV such as scheduling instruction streams based on priority (thereby allowing to get more important processes completed quicker) in any system and not just in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.
14a) invention XIV has separate utility from invention XV such as scheduling instruction streams based on priority (thereby allowing to get more important processes completed quicker) in any system and not just in a system which has a controller for transferring data to/from internal processing element memory independent of processor element operation.

See MPEP § 806.05(d).

***Telephone Restriction Practice***

3. Section 812.01 of the Manual of Patent Examining Procedure (MPEP) states the Examiner does not have to telephone the attorney or agent in cases where the Restriction is deemed complex. The Restriction is deemed complex by the Examiner and the attorney/agent should be afforded the benefit of receiving the action for careful review and time to formulate a response.

*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
February 6, 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100